Substitute for Form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

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Complete if Known	
Application Number	09/843,486
Filing Date	
First Named Inventor:	
Art Unit	2811
Examiner Name	
Attorney Docket Number	004363.P004

Sheet 1 of 4

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
qv		US-	6,578,179 B2	06-10-2003	Shirotori, et al.	
qv		US-	6,574,786 B1	06-03-2003	Pohlenz, et al.	
qv		US-	6,539,533 B1	03-25-2003	Brown, III et al.	
qv		US-	6,581,188	06-17-2003	Hosomi, et al.	
qv		US-	6,311,315	10-30-2001	Tamaki	
qv		US-	6,002,860	12-14-1999	Voinigescu, et al.	
qv		US-	5,754,826	05-19-1998	Gamal, et al.	
qv		US-	5,633,807	05-27-1997	Fishburn, et al.	
qv		US-	5,055,716	10-08-1991	El Gamel	
qv		US-	5,289,021	02-22-1994	El Gamel	
qv		US-	4,827,428	05-02-1989	Dunlop, et al.	
		US-				
		US-				
		US-				
		US-				

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
qv		WO 01/37429 A1	05-25-2001	HORAN, et al.		

Examiner Signature		Date Considered	07/19/05

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Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	09/843,486
				Filing Date	4-25-01
				First Named Inventor:	Arash Hassibi, et al.
				Art Unit	2811
				Examiner Name	Quang D. Vu
Sheet	2	of	4	Attorney Docket Number	004363.P004

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
qv		HERSHENSON, M., et al., "Automated Design of Folded-Cascode Op-Amps with Sensitivity Analysis", pp. 121-124, Electronics, Circuits and Systems, IEEE International Conference on LISBOA, September 7-10, 1998.	
qv		HERSHENSON, M., et al., "GPCAD: A Tool for CMOS Op-Amp Synthesis" 8 pages, Proceedings of the IEEE/ACM International Conference on Computer Aided Design (ICCAD), pp. 296-303, November 1998.	
qv		HERSHENSON, M., et al., "Posynomial models for MOSFETs" 9 pages, July 7, 1998.	
qv		CHANG, H, et al., "A Top-Down, Constraint-Driven Design Methodology for Analog Integrated Circuits" 6 pages, IEEE 1992 Custom Integrated Circuits Conference.	
qv		CHAVEZ, J., et al, "Analog Design Optimization: A Case Study" 3 pages, IEEE, January 1993.	
qv		KORTANEK, K.O., et al., "An Infeasible interior-point algorithm for solving primal and dual geometric programs" pp. 155-181, Mathematical Programming 76 (1996).	
qv		GEILEN, G., et al., "Analog Circuit Design Optimization Based on Symbolic Simulation and Simulated Annealing", pp. 707-713, IEEE Journal of Solid-State Circuits, Vol. 25, No. 3, June 1990.	
qv		FISHBURN, J, et al., "TILOS: A Posynomial Programming Approach to Transistor Sizing" pp. 326-328, IEEE, 1985.	
qv		MAULIK, P., et al., "Integer Programming Based on Topology Selection of Cell-Level Analog Circuits", 12 pages, IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 14, No. 4, April 1995.	
qv		SWINGS, K., et al., "An Intelligent Analog IC Design System Based On Manipulation Of Design Equations" pp. 8.6.1- 8.6.4, IEEE 1990, Custom Integrated Circuits Conference.	
qv		NESTEROV, Y., et al., "Interior-Point Polynomial algorithms in Convex Programming" 8 pgs., 1994, Society for Industrial and Applied mathematics.	

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Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	09/843,486
				Filing Date	4-25-01
				First Named Inventor:	Arash Hassibi, et al.
				Art Unit	2811
				Examiner Name	Quang D. Vu
Sheet	3	**of**	4	Attorney Docket Number	004363.P004

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
qv		YANG, H.Z., et al., "Simulated Annealing Algorithm with Multi-Molecule: an Approach to Analog Synthesis" pp. 571-575, IEEE, 1996,	
qv		WONG, D.F., et al., "Simulated Annealing For VLSI Design" 6 pages, 1998, Kulwer Academic Publishers.	
qv		MAULIK, P., et al., "Sizing of Cell-Level Analog Circuits Using Constrained Optimization Techniques" pp. 233-241, IEEE Journal of Solid-State Circuits, Vol. 28, No. 3, March 1993.	
qv		OCHOTTA, E, et al., "Synthesis of High –Performance Analog Circuits in ASTRX/OBLS" pp. 273-295, IEEE Transactions on Computer-Aided Design of Integrated Circuits And Systems, Vol. 15, No. 3, March 1996.	
qv		WRIGHT, S., "Primal-Dual Interior-Point Methods" pp. 1-3, http://www.siam.org/books/wright, Printed August 19, 1998	
qv		SHYU, J., et al., "Optimization-Based Transistor Sizing" pp. 400-408, IEEE Journal of Solid-State Circuits, Vol. 23, No. 2, April 1998.	
qv		WRIGHT, S., "Primal-Dual Interior-Point Methods" 14 pages, 1997, Society for Industrial and Applied Mathematics.	
qv		VAN LAARHOVEN, P.J.M., et al., "Simulated Annealing: Theory and Applications" 26 pages, 1987, Kulwer Academic Publishers.	
qv		HERSHENSON, M., et al., "CMOS Operational Amplifier Design and Optimization via Geometric Programming" pp. 1-4, Analog Integrated Circuits, Stanford University.	
qv		AGUIRRE, M.A., et al., "Analog Design Optimization by means of a Tabu Search Approach" pp. 375-378.	
qv		MEDEIRO, F., et al., "A Statistical Optimization-Based Approach for Automated Sizing of Analog Cells", pp. 594-597, Dept. of Analog Circuit Desing.	

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				Art Unit	2811
				Examiner Name	Quang D. Vu
Sheet	4	of	4	Attorney Docket Number	004363.P004

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NON PATENT LITERATURE DOCUMENTS

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qv		SPATNEKAR, S., "Wire Sizing as a Convex Optimization Problem: Exploring the Area-Delay Tradeoff" 27 pages, Dept. of Electrical and Computer Engineering.	
qv		SU, H., et al., "Statistical Constrained Optimization of Analog MOS Circuits Using Empirical Performance Models" pp. 133-136.	
qv		VASSILIOU, I., et al, "A Video Driver System Designed Using a Top-Down, Constraint-Driven Methodology" 6 pages.	
qv		SAPATNEKAR, S, et al., "An Exact Solution to the Transistor Sizing Problem for CMOS Circuits Using Convex Optimization" 35 pages.	

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Based on Form PTO/SB/08B (08-03) as modified by BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP on 09/10/03.